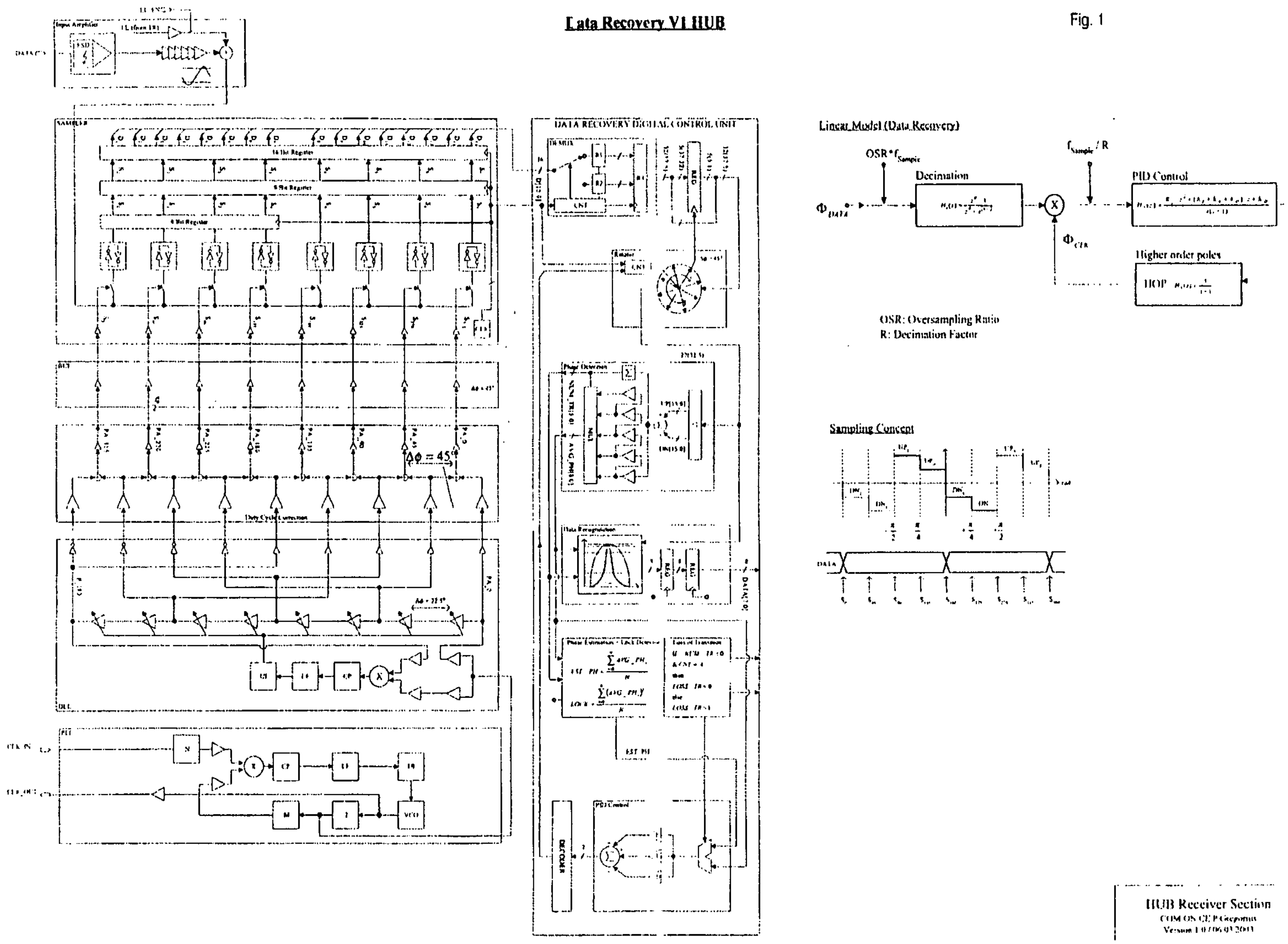
Fig. 1



HUB Receiver Section
COM ON CE P Gregorius
Version 1.0 / 06.03.2003

Fig. 2

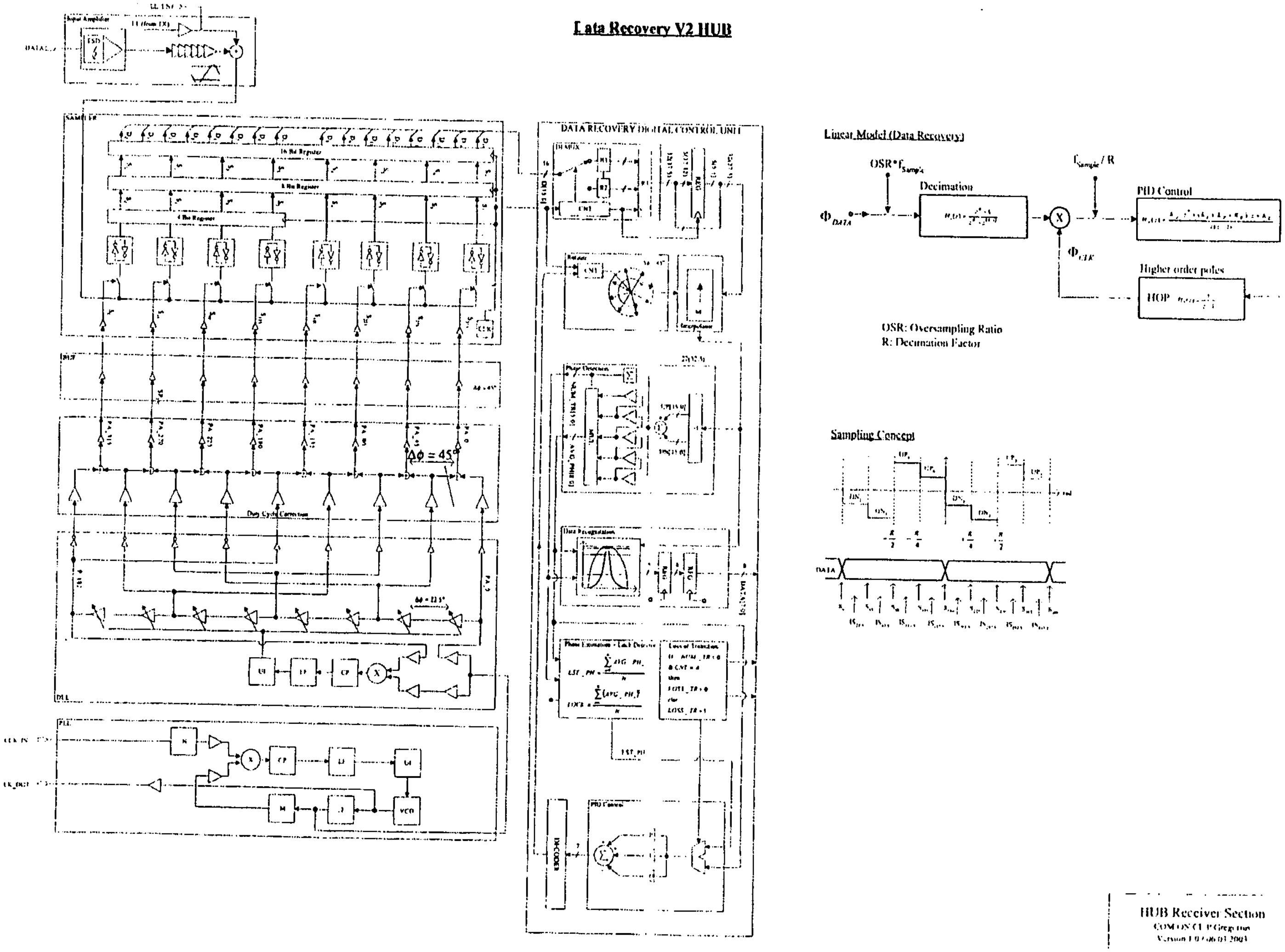

Lata Recovery V2 HUB
DATA RECOVERY DIGITAL CONTROL UNIT
Input Amplifier
DATA
16 Bit Register
8 Bit Register
4 Bit Register
CLK
Δφ = 45°
Duty Cycle Correction
DLL
PLL
VCO
DECODER
PID Control
Phase Detection
Data Recognition
REG
CNT
EST_PH
Linear Model (Data Recovery)
OSR*f_Sample
Decimation
f_Sample / R
PID Control
Φ_DATA
Φ_CLK
Higher order poles
HOP
OSR: Oversampling Ratio
R: Decimation Factor
Sampling Concept
DATA
HUB Receiver Section
COMLOS CLP Gregorios
Version 1.0 / 06.03.2003

Fig. 3

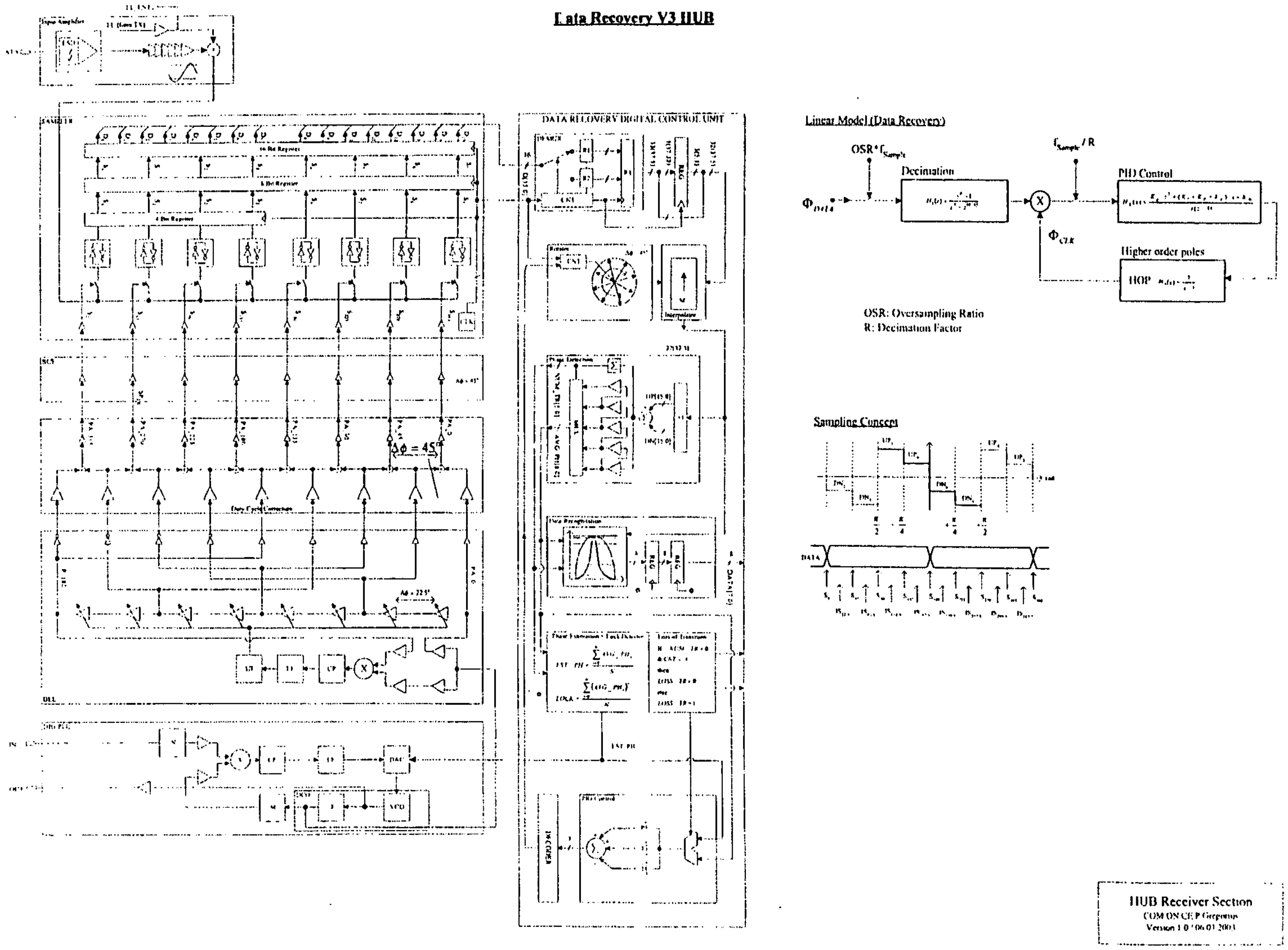
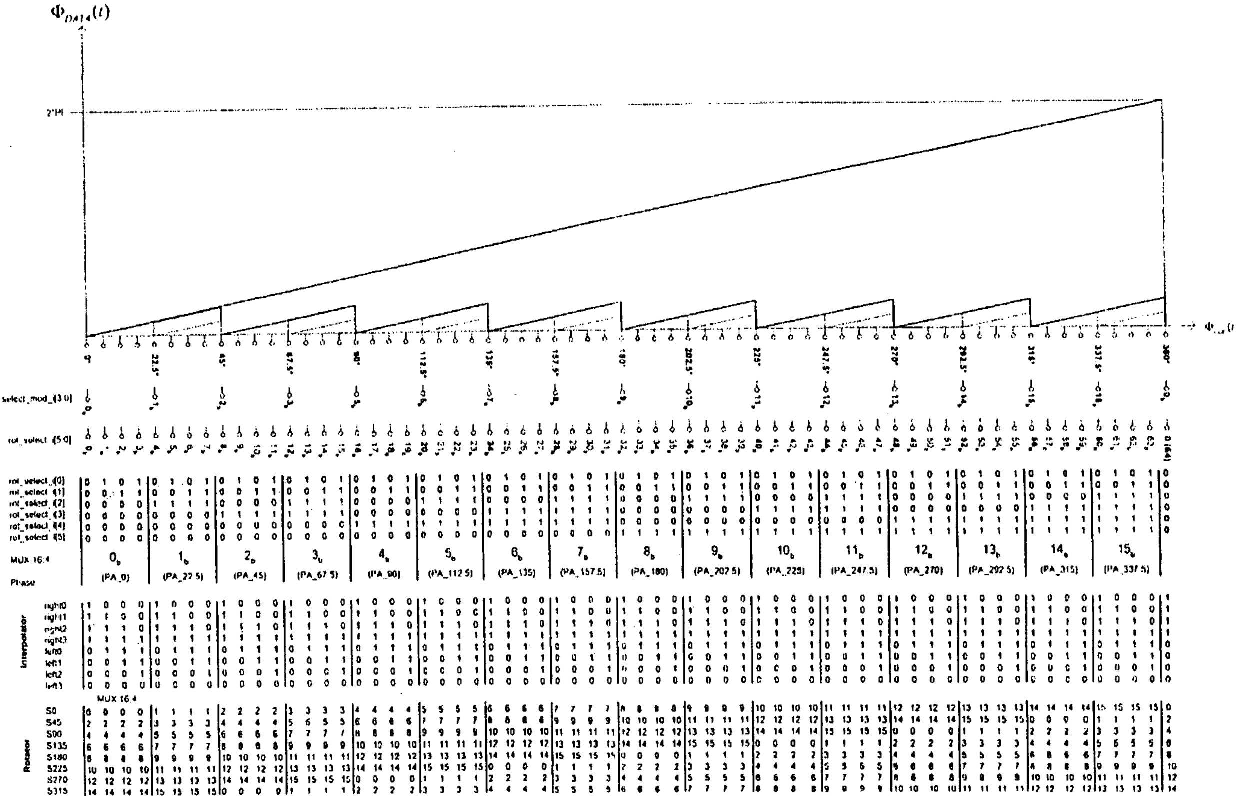

Lata Recovery V3 HUB
DATA RECOVERY DIGITAL CONTROL UNIT
REG
CNT
Interpolator
Phase Detection
Data Recognition
DATA[7:0]
EST_PH
DECODER
Duty Cycle Correction
Δφ = 45°
Δφ = 22.5°
DLL
SAMPLER
VCO
DAC
Linear Model (Data Recovery)
OSR*f_Sample
Decimation
f_Sample / R
PID Control
Φ_DATA
Φ_CLK
Higher order poles
HOP
OSR: Oversampling Ratio
R: Decimation Factor
Sampling Concept
DATA
HUB Receiver Section
COM ON CE P Gregorius
Version 1.0 / 06.01.2003

Fig. 4

Decoder (Interpolator & Rotator)HUB

HUB Receiver Section
COM ON CE P.Gregorius
Version 1.0 / 06.03.2003



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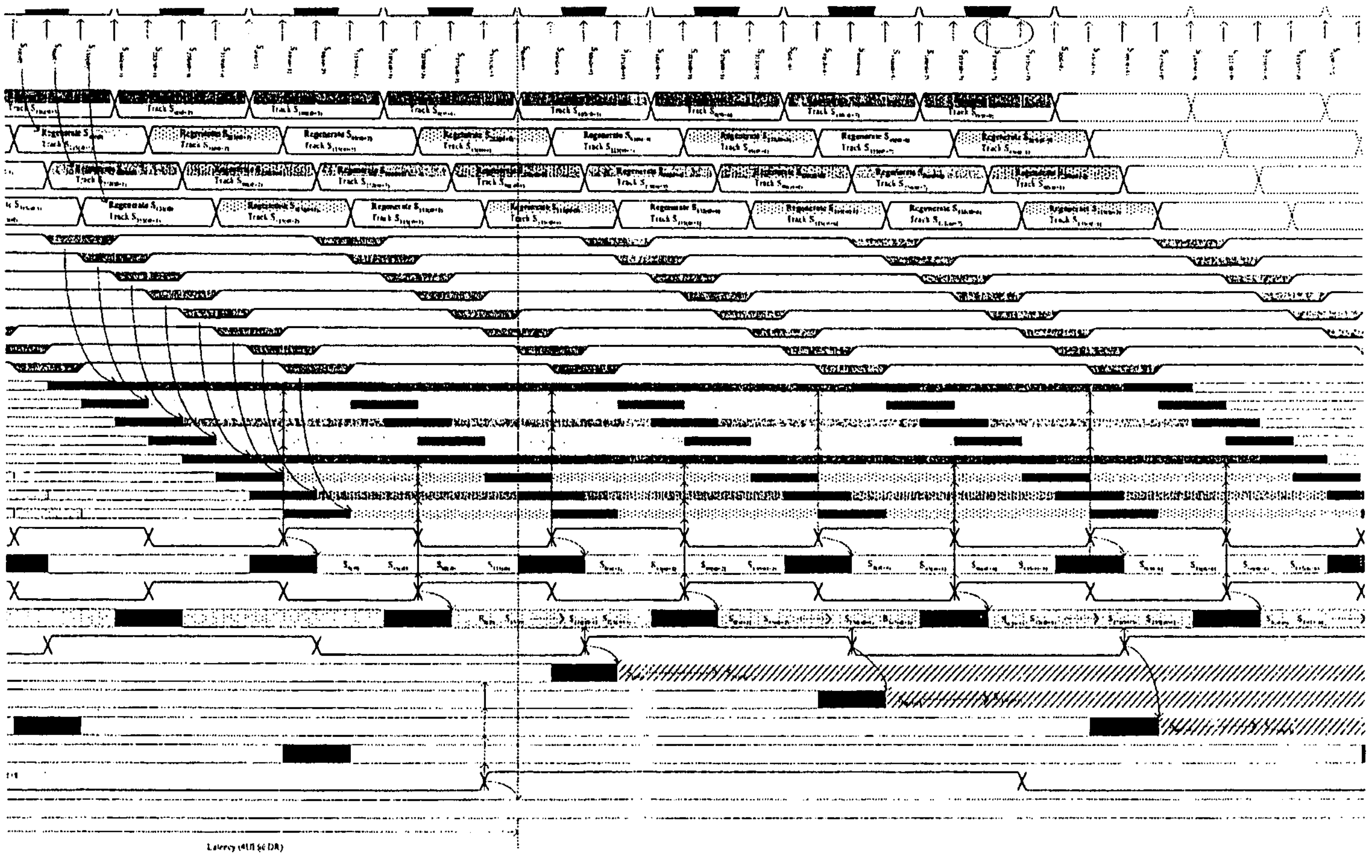

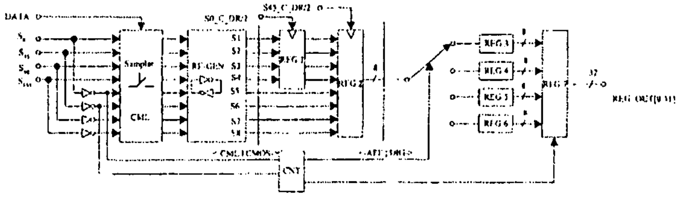

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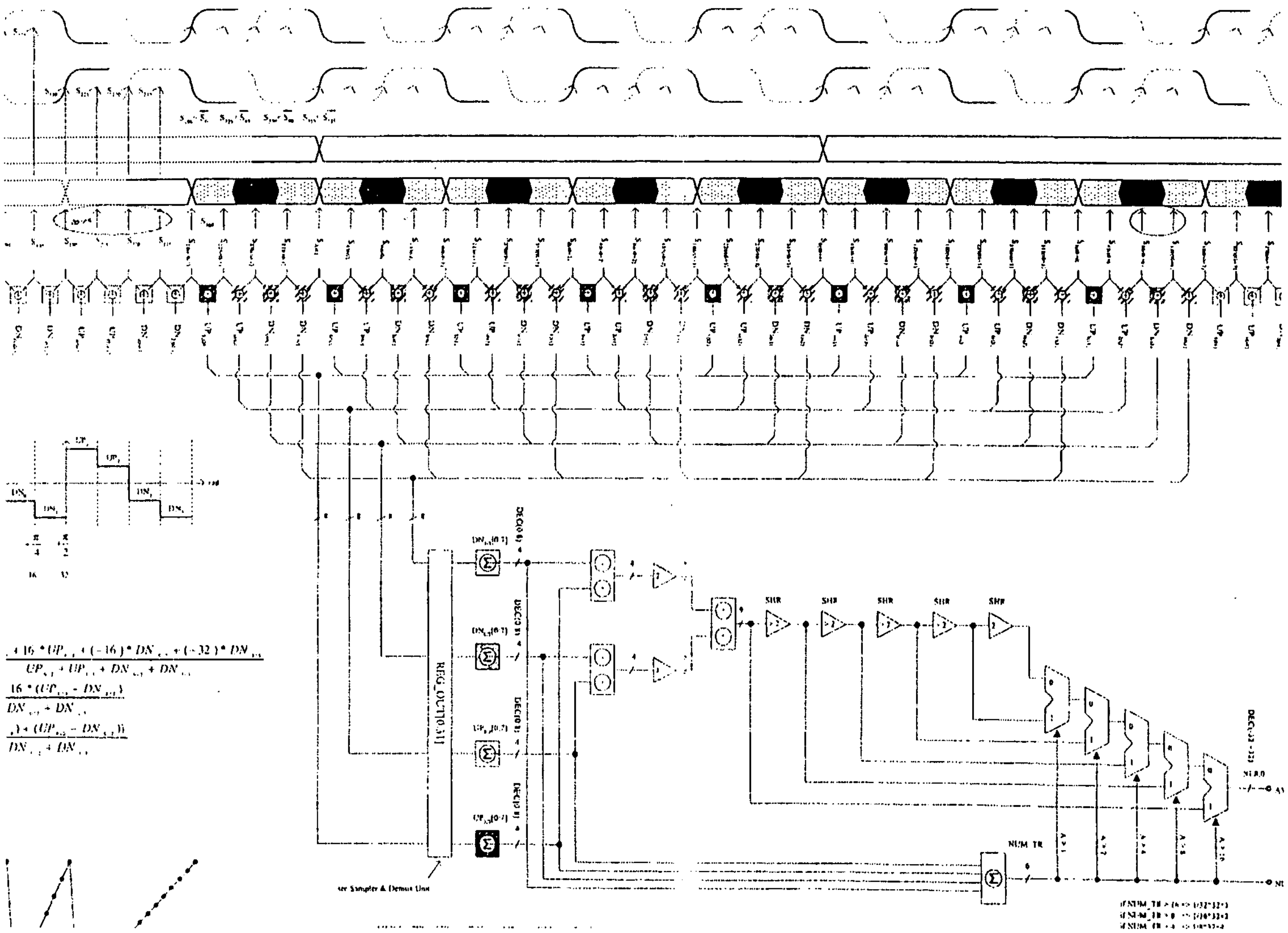
Half Rate Phase Detection Algorithm (Timing Recovery)



Data Recognition Unit (Timing Recovery)